International Journal of Computer Science & Communication (ISSN: 0973-7391)
Volume 13 • Issue 2 pp. 33-39 March- Sept 2022 www.csjournals.com

# Improved Design of Two Stage CMOS Operational Amplifier for high CMRR

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**Abstract:** In this paper a method is presented for the two-stage CMOS operational amplifier design, the amplifier that has to reduces the noise on the transmission lines, increase the gain and improve stability. The two-stages of Op-Amp is made up of a Differential Amplifier as the initial stage, followed by a second stage Common Source amplifier. By connecting a capacitor in series with a resistor between the second stage amplifier's input and output, the Op-Amp is compensated. This approach leads to a noticeable improvement in the gain, CMRR and phase margin, providing the ability to give high gain, reject common-mode signals and improved stability.

**Keyword:** Gain, CMRR, Unity gain frequency, Phase Margin.

## 1. INTRODUCTION

Fundamentally, an amplifier is a device that increases input signal strength and is intended to be operated in combination with external feedback elements between its output and input terminals, such as resistors and capacitors [1]. The general term "amplifier" is used to describe a circuit that produces a more powerful version of its input signal. Due to its capacity to amplify a relatively weak input signal, small signal amplifiers are frequently used devices. The operational amplifier studied, often known as an OpAmp, is a high-gain electronic voltage amplifier with differential input and that mostly has a single-ended output. The main goal of operational amplifier is to provide better amplification along with high CMRR and greater phase margin for stability of amplifier [2-6]. With the right choice of the components and their values, the OpAmp can be used as a current to voltage converter, active rectifier, integrator, comparators, voltage follower, Differentiators, summing amplifier. Ideally an OpAmp should have infinite input resistance, infinity voltage gain, and zero output resistance [7].

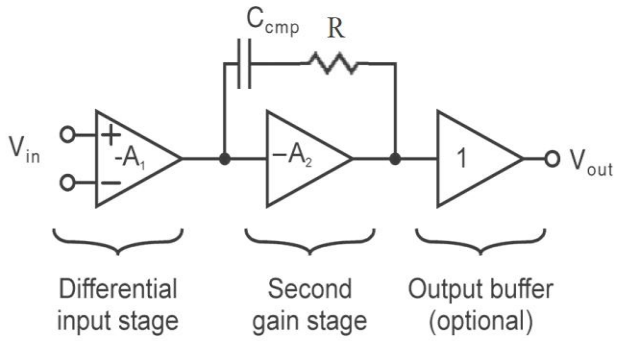


**Figure 1: Block Diagram of two stage CMOS Op-Amp**

As shown in figure 1, a block model of a typical two-stage Operational Amplifier is displayed. The term "two stages" refers to the Op-Amp's two gain stages. The three amplifiers in figure 1 are actually two gain amplifiers i.e. the first and second amplifier and the third amplifier is a unity-gain output amplifier often known as buffer. The third amplifier i.e., buffer is typically only needed to drive resistive loads. It is rarely provided if the load is purely capacitive.

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A 2-stage Op-Amp generally consists of three amplifier, namely:

a) Differential-input single-ended output amplifier.
b) The Common-Source amplifier output stage serves as the second gain stage.
c) Buffer stage.

## 2. DESIGN PROCEDURE

As shown in figure 2, the first stage of the schematic for a two-stage operational amplifier is an NMOS differential amplifier (MOSFET $M_1$ and $M_2$) with an active load PMOS current mirror ($M_3$ and $M_4$ MOSFET). The Op-Amp second stage is a common-source PMOS amplifier (MOSFET $M_6$), in which $M_6$ acts as an amplifier and $M_7$ acts as the current source for biasing. MOSFET $M_5$ and $M_8$ work together to create an NMOS current mirror, which is utilized to bias the circuit and provide the proper current and voltages.

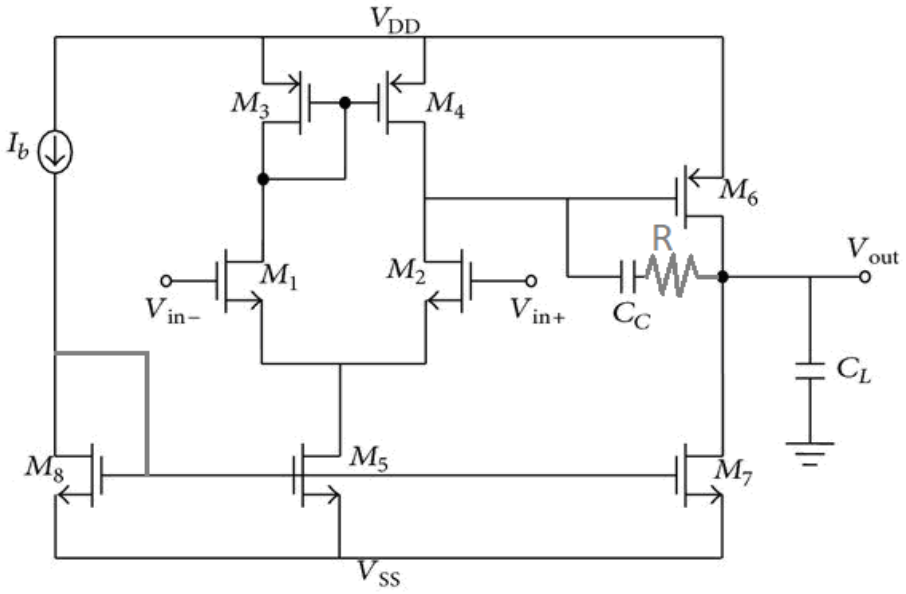


**Figure 2: Circuit diagram of two stage CMOS operational amplifier**

A feedback capacitor Cc that is connected between the second stage amplifier's input and the second stage amplifier's output is used as a miller capacitance to obtain pole splitting (increasing the distance between the first and second pole) and that will provide better stability, along with capacitor Cc a resistor R that is called as nulling resistor and is connected in series with capacitor Cc to provide greater phase margin to achieve greater stability. With the nulling resistor, we can move the RHP (right half plane) zero to infinity. In this simulation we have chosen resistor R such that the RHP zero moves towards infinity or practically we can say towards a very higher frequency.

### 2.1 Gain

The ratio of the output voltage to the input voltage is known as gain. Gain is frequency dependent. An ideal amplifier has infinite gain. Gain is referred to as closed loop gain if there is any feedback connection between the amplifier's output and input; otherwise, it is referred to as open loop gain. The bode plot is used to define the signal gain and phase with respect to frequency.

$$\text{Gain} = \frac{V_{out}}{V_{in}}$$

### 2.2 Phase Margin

Phase Margin of a system is defined to ensure the stability of a system. To increase the stability of an amplifier phase margin should be increased. The phase margin is calculated from bode phase plot, it is the value of the phase at a frequency known as the gain crossover frequency, where the gain is 0 dB.

$$PM = \phi - (-180^{o}): \quad \text{where } \phi < 0^{o}$$

### 2.3 CMRR

The CMRR (common mode rejection ratio) of a device is used to measure how well it can reject common-mode signals, those signals that occur simultaneously and in-phase on both inputs. A differential amplifier's CMRR should ideally be infinite.

An Op-Amp should only amplify differential input voltage, common-mode output voltages must not be visible at the output. However, some common-mode voltage $V_{OCM}$ will be visible at the output due to flaws in an actual Op-Amp.

Practically, In equation form,

$$A_{CM} = \frac{V_{OCM}}{V_{CM}}$$

Generally, the ratio of the differential gain $A_D$ to the common-mode gain $A_{CM}$, also known as CMRR is used to describe this phenomenon:

$$CMRR = \frac{A_D}{A_{CM}}$$

Using above two equations, we can determine the connection between the $V_{OCM}$ and CMRR:

$$CMRR = \frac{A_D}{A_{CM}} = \frac{A_D}{V_{OCM} / V_{CM}}$$

$$CMRR = \frac{A_D * V_{CM}}{V_{OCM}}$$

Above equation shows that smaller the value of output voltage ($V_{OCM}$) amplitude that is generated by common-inputs, higher the value of CMRR.

CMRR in decibels (dB):

$$CMRR \text{ in dB} = 20\log\frac{A_D}{A_{CM}}$$

Thus greater CMRR Op-Amp's should be used because they have a superior ability to reject common-mode voltage.

**Table 1: Different components and their values**

| Components | Values |
|---|---|
| $V_{DD}$ | 1.2 V |
| R | 3.4 kΩ |
| $C_C$ | 4.5 pF |
| $C_L$ | 10 pF |
| $V_{in}^{+}$ | DC= 1 Volt : AC= -1 Volt |
| $V_{in}^{-}$ | DC= 1 Volt : AC= 1 Volt |
| $V_{SS}$ | 0 Volt |

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**Table 2: Width and Length of all the MOSFET**

| Mosfet's | Practical values (W) | Practical values (L) |
|---|---|---|
| $M_1$, $M_2$ | 11µ | 1µ |
| $M_3$, $M_4$ | 10µ | 1µ |
| $M_5$. $M_8$ | 8µ | 1µ |
| $M_6$ | 50µ | 1µ |
| $M_7$ | 20µ | 1µ |

## 3. SIMULATION OF PROPOSED DESIGN

Make the connections as shown in the figure 3. Put in the component values and mosfet parameter values (W and L) as shown in tables 1 and 2, respectively.

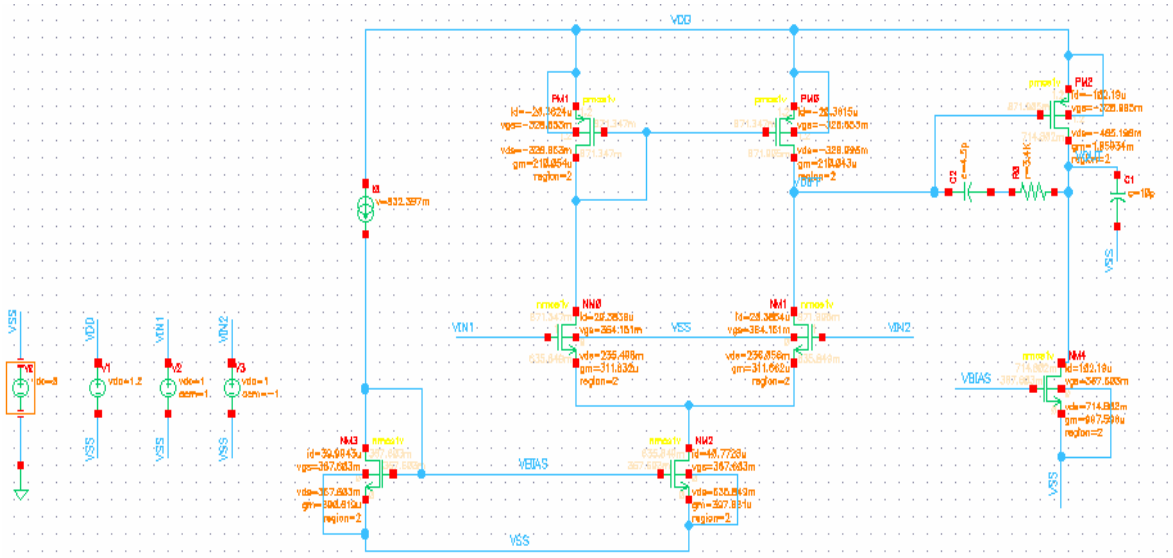


**Figure 3: Two stage CMOS Op-Amp Schematic**

The schematic of a two stage differential and common mode Op-Amp input is shown in figure 4(a) & 4(b)

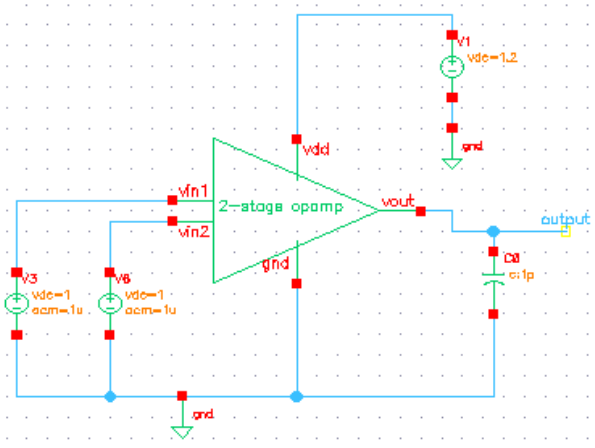


**Figure 4(a): A 2-stage Operational Amplifier with differential input**

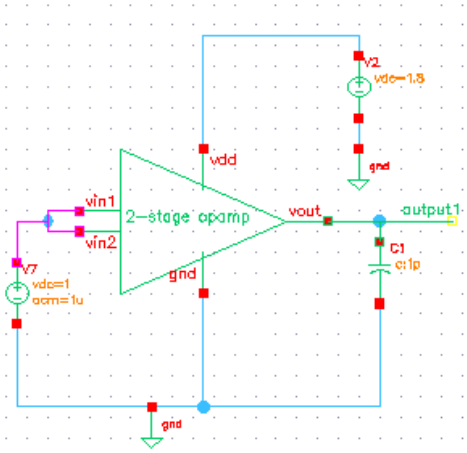


**Figure 4(b): A 2-stage Operational Amplifier with common input**

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## 4. RESULTS AND DISCUSSION

In this section, the results of AC and DC simulations are presented, along with a discussion of the proposed two-stage operational amplifier. With 90nm technology, a wide variety of frequencies were covered while simulating and inspecting the OpAmp using the cadence virtuoso EDA tool.

As shown in Figure 5, the graph of phase in degree and gain in dB shows that the gain is of 82 dB at M91 mark and the unity gain frequency at 0dB is 22.6228 MHz at M92 mark. The previous result for gain was 72 dB and now it is 82 dB which is increased by 10 dB, which is an increment of 13% from the previous value [16]. The phase margin at mark M93 where the gain bandwidth product is 22.6228 Mhz comes to be $69^{o}$. The previous result for phase margin was $61^{0}$ and now it is $69^{o}$ which is increased by $8^{o}$, which is an increment of 13% from the previous value [16].

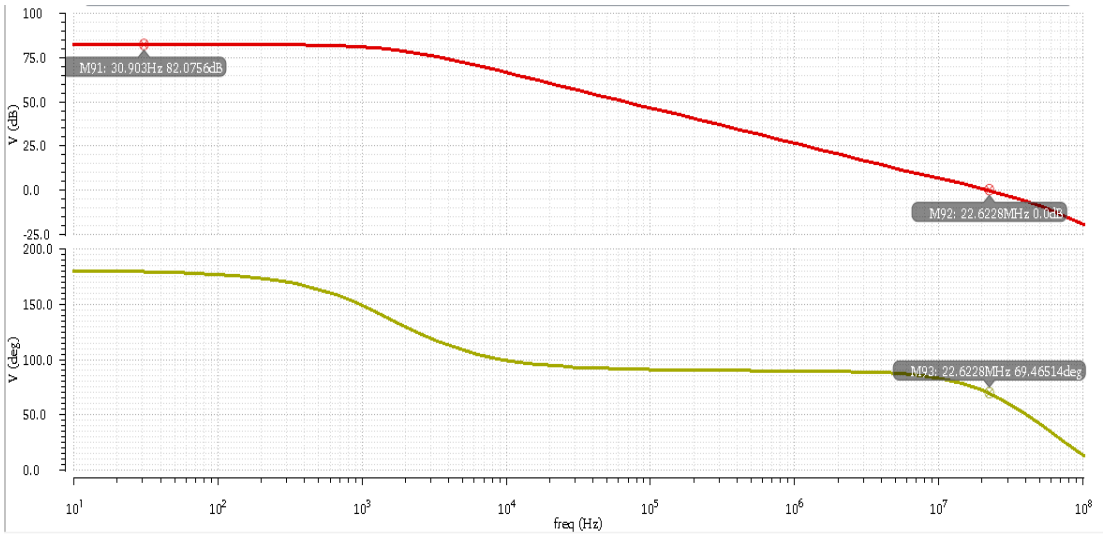


**Figure 5: Gain & Phase Plot for Op-Amp**

As shown in figure 6, the CMRR comes to be 86dB. The previous result for CMRR was 60dB and now it is 86dB which is increased by 26dB, which is an increment of 43% from the previous value [16].

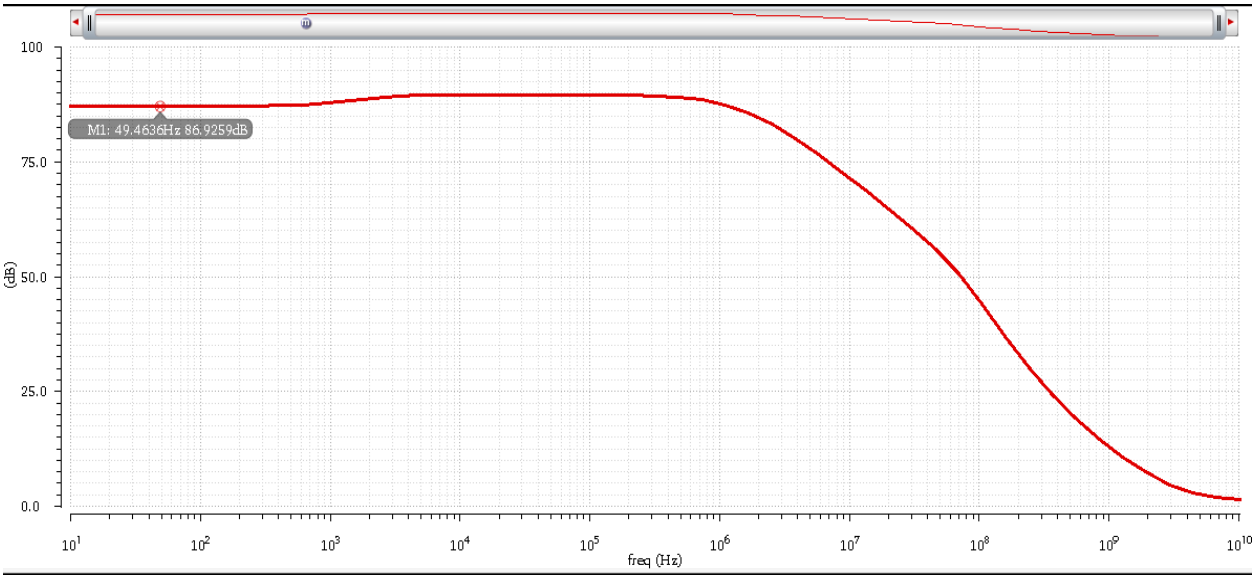


**Figure 6: The CMRR waveform of two stage Op-Amp**

**Table 3: Comparison between previous and proposed result.**

| Parameters | Previous Results[16] | Proposed Results | Improvement |
|---|---|---|---|
| Gain | 72 dB | 82 dB | Increased by 13 % |
| Phase Margin | $61^o$ | $69^o$ | Increased by 13 % |
| CMRR | 60 dB | 86 dB | Increased by 43% |
| Unity Gain Frequency | 16.6 MHz | 22.6 MHz | Increased by 10 MHz |

The results of the 90 nm technology-based simulation of a two-stage CMOS operational amplifier are much better than those of the earlier simulation. Table 3 shows that the gain and phase margin is raised by 13%, and the CMRR is increased by 43%. As a result, the operational amplifier's gain, stability and CMRR increased, making the amplifier more stable and noise-tolerant.

## 5. CONCLUSION

To overcome the stability issue that second order system experience, the integrated circuit system is made to behave like single-pole systems over a broad frequency range. To fulfill the demands of the design specification, the Miller compensating approach is used. The gain comes to be 82 dB and the CMRR has been increased and obtain a value of 86 dB. This Op-Amp circuit is suitable for high performance. The unity gain frequency comes to be 22.6228 MHz. The phase margin of Op-Amp comes to be 69° which makes the proposed operational amplifier appropriate for greater stability, higher amplification and it has ability of better tolerance against noise.

## REFERENCE

[1] Boaz Shem-Tov, Mucahit Kozak, and Eby G. Friedman, “A High Speed CMOS Op-Amp Design Techniques using Negative Miller Capacitance,” proceedings of the 11th IEEE International Conference on Electronics, circuit and systems, December 2004.

[2] F Aziz, N Ahmad and F A S Musa, “90nm Two-Stage Operational Amplifier Using Floating-gate MOSFET”, 4th Electronic and Green Materials International Conference 2018 (EGM 2018), December 2018,AIP Publishing. 978-0-7354-1771-7/$30.00

[3] Kanika Sharma, Rahil Kumar, “Design of a Two Stage CMOS operational amplifier using 180nm and 90nm technology”, International Journal of Advanced Research in Electrical Electronics and Instrumentation Engineering, Vol. 5, Issue 5, May 2016.

[4] Sumukh Nitundil,,Nihal Singh, Rushabha Balaji, Pankaj Arora, “Design and Comparative analysis of a Two-Stage Ultra-Low-Power Subthreshold Operational Amplifier in 180nm, 90nm, and 45nm technology”, 2021 Devices for Integrated Circuit (DevIC), 19-20 May 2021, **DOI:** 10.1109/DevIC50843.2021.9455791.

[5] S. S. Rajput, A. Singh, A. K. Chandel, and R. Chandel, “Design of Low-Power High-Gain Operational Amplifier for Bio-Medical Applications,” in 2016 IEEE Computer Society Annual Symposium on VLSI, 2016, pp. 355–360.

[6] K. A. Ng and Y. P. Xu, “A Low-Power , High CMRR Neural Amplifier System Employing CMOS Inverter-Based OTAs With CMFB Through Supply Rails,” IEEE JOURNAL OF SOLID-STATE CIRCUITS, vol. 51, no. 3, pp. 724–737, 2016.

[7] C. Yadav and S. Prasad, “Low Voltage Low Power Sub-threshold Operational Amplifier in 180nm CMOS,” in 2017 Third international conference on sensing, signal processing and security (ICSSS), 2017, pp. 35–38.

[8] J. Magri, I. Grech, O. Casha, E. Gatt, and J. Micallef, “Design of CMOS Front-End Circuitry for the Acquisition of Biopotential Signals,” in 2016 IEEE International Conference on Electronics, Circuits and Systems (ICECS), 2016, pp. 161–164.

[9] K. N. Abhilash, S. Bose and A. Gupta, "A high gain, high CMRR two-stage fully differential amplifier using gm/Id technique for bio-medical applications," 2013 IEEE Asia Pacific Conference on Postgraduate Research in Microelectronics and Electronics (PrimeAsia), Visakhapatnam, India, 2013, pp. 40-45, doi: 10.1109/PrimeAsia.2013.6731175.

[10] B. Razavi, “Design of Analog CMOS Integrated Circuits”, New York: Mc-Graw Hill, 2001 .

[11] D. Johns and Ken Martin, “Analog Integrated Circuit Design”, Wiley India Pvt. Ltd, 1997.

[12] Henil Langalia, Sarthak Lad, Mangesh Lolge and Surendra Rathod, "Analysis of two-stage CMOS Op-Amp for Single- Event Transients" International Conference on Communication, Information & Computing Technology (ICCICT), Oct. 19-20,2012, Mumbai, India, pp. 1-4.

[13] Sunil M.P and Hari Krishna Murthy, "Design and Implementation of 90dB-4mW Two Stage CMOS Operational Amplifier Using 180nm" 3rd International Conference on Electronics and Communication Systems (ICECS-2016) 25-26th, February 2016, Coimbatore, Tamilnadu, India

[14] C. L. Kavyashree, M. Hemambika, K. Dharani, A. V. Naik and M. P. Sunil, "Design and implementation of two stage CMOS operational amplifier using 90nm technology," 2017 International Conference on Inventive Systems and Control (ICISC), 2017, pp. 1-4, doi: 10.1109/ICISC.2017.8068601.

[15] D. Tripathy and P. Bhadra, "A High Speed Two Stage Operational Amplifier with High CMRR," 2018 3rd IEEE International Conference on Recent Trends in Electronics, Information & Communication Technology (RTEICT), Bangalore, India, 2018, pp. 255-259, doi: 10.1109/RTEICT42901.2018.9012268.

[16] Ranjan, Praful & Dhaka, Nitin & Pant, Ishan & Pranav, Ashutosh. (2017) "Design and Analysis of Two Stage Op-Amp for Bio-Medical Application" International Journal of Wearable Device. 3. 9-16. 10.21742/ijwd.2016.3.1.02.